7.2.40.11 Sub-Register 0x27:28 – DRX_CAR_INT

ID	Length (octets)	Type	Mnemonic	Description
27:28	3	RO	DRX_CAR_INT	Carrier Recovery Integrator Register

Register file: 0x27 – Digital receiver configuration, sub-register 0x28 is a read-only 21 bit register.

The DW1000 receiver needs to compensate for frequency offsets between the timing references at the transmitting device and itself to successfully receive a packet. Therefore, when a packet is successfully received, the DW1000 has a sufficiently accurate estimate of the frequency offset.

This information is available in the carrier recovery integrator register, at address 0x27, offset 0x28. This is a 21 bit number with the lower 17 bits, the fractional part, and the upper 4 bits as the integer portion of the number.

When a packet is successfully received, this register can be read and converted to the frequency error (in Hz) using

$$F_{offset} = \frac{C_{int} \times 2^{-17}}{2\left(\frac{N_{samples}}{F_s}\right)}$$

$$\begin{aligned} &where \\ C_{int} &= carrier\ integrator\ value \\ N_{samples} &= \begin{cases} 8192\ for\ 110kb/s \\ 1024\ otherwise \end{cases} \\ F_s &= 998.4 \times 10^6 \end{aligned}$$

F_{offset} is the absolute frequency error in Hz. It can be converted to a clock offset (in ppm) by scaling by the carrier frequency as follows

$$Offset_{ppm} = -10^6 \times \frac{F_{offset}}{F_c}$$

$$\begin{aligned} &where \\ F_{offset} &= frequency\ offset\ in\ Hz \\ F_c &= 6489.6MHz\ for\ channel\ 5 \end{aligned}$$

The minus sign is produced by the process of measuring the clock offset.

For a particular channel, the formulas reduce to multiplying the content of the carrier integrator register with the appropriate constant from the table below:

Table 35: Constants for frequency offset calculation

Data Rate	Channel 2	Channel 3	Channel 5
850 kb/s, 6.81 Mb/s	-0.9313e-3	-0.8278e-3	-0.5731e-3
110 kb/s	-0.1164e-3	-0.1035e-3	-0.0716e-3