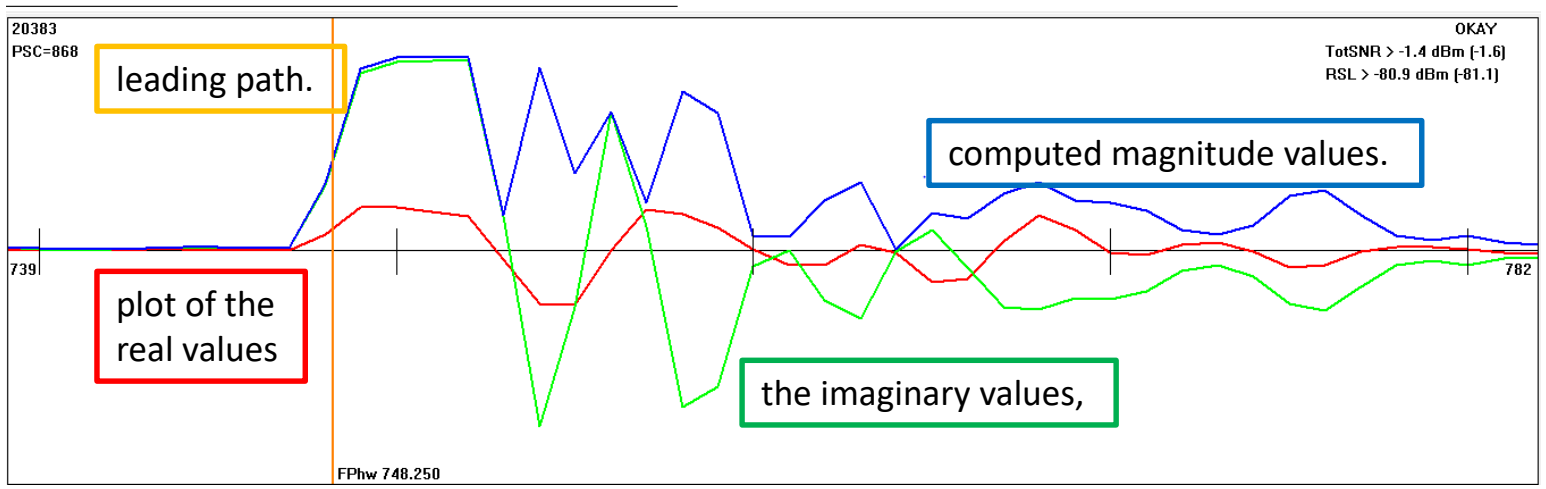
The channel response is an array of complex values, the red line is the plot of the real values, the green line is the imaginary values, and the blue line is the computed magnitude values. This graphing shows the DW1000's view of the channel impulse response. The graphic also indicates with a vertical orange line where the DW1000 finds the leading path.

In the Anchor Side with the help of DecaRanging Application, it is possible to see the CIR in real time. When you pause it, the system gives a possibility to take a log sample with the information regarding CIR (Found in Accumulator Register (0x25)). Also there is an option to read the register values from the DW1000 at the same time.

Preamble symbol count -See DW1000 User Manual symbol: RXPACC (part of register 0x10)



FP_INDEX - See register 0x15 in DW1000 User Manual:

We start around 750. This has to do with the research we did in this area and based on the investigation we decided to design the chip algorithm to locate the bulk of the channel between index 728 and 855 of the CIR memory. So the first path tends to end up around 740.

TotSNR is derived from RSL, SNR = RSL + delta.

Receive Signal Level –
See DW1000 User Manual section (4.7.2 Estimating the receive signal power)
The value in brackets is average of last 10 values

Other relevant documentation:

- APS006 part 1 channel effects on range accuracy
- APS006_Part2 NLOS Operation and Optimizations
- APS006 Part 3 DW1000 Diagnostics for NLOS Channels
- APS011 Sources of error in TWR
- PC Decaranging Source Code**

All available from: https://www.decawave.com/support
** Available at request

FOLLOWING TEXT IS TAKEN FROM PC DECARANGING USER MANUAL

The top-left number 20383) is an indication of the height of display max-amplitude. The **PSC** number indicates the number of preamble symbols accumulated. The numbers below the mid line (**739 & 782**) are accumulator index (nanosecond) values, while the **FPhw** value beside the orange line is the DW1000 IC reported leading path (sub-nanosecond) position. The **SNR** and **RSL** values are calculated from diagnostic values reported by the DW1000 (please refer to the DW1000 user manual for more details ofthese). Moving average of the last 10 values is reported beside their instantaneous value as shown in Figure 18.

Decaranging Log Channel Responses

C5 13 Rx time = 8.226938816481371e-001 0C3D4E88DC

C5 13 **Rx time(un)** = 8.226941185897436e-001 0C3D4EC400

txdly 4034 rxdly 4034
RX DATA: c5137510605e20990910b222

RX OK WInd(0735), HLP(0747.3750), PSC(0108), SLP(0000.0000), RC(000C 3D4E88DC), DCR(0), DCI(0), NTH(016A), T(6CBE), RSL(-099.7722), FSL(-100.0241), RSMPL(3F)
Accum Len 1016
12, -32
13, -13
-22, 64
3, 50
-41, 82
-17, 78
59, 63
[...]
44, 59
22, 44
13, -17

[TXD]

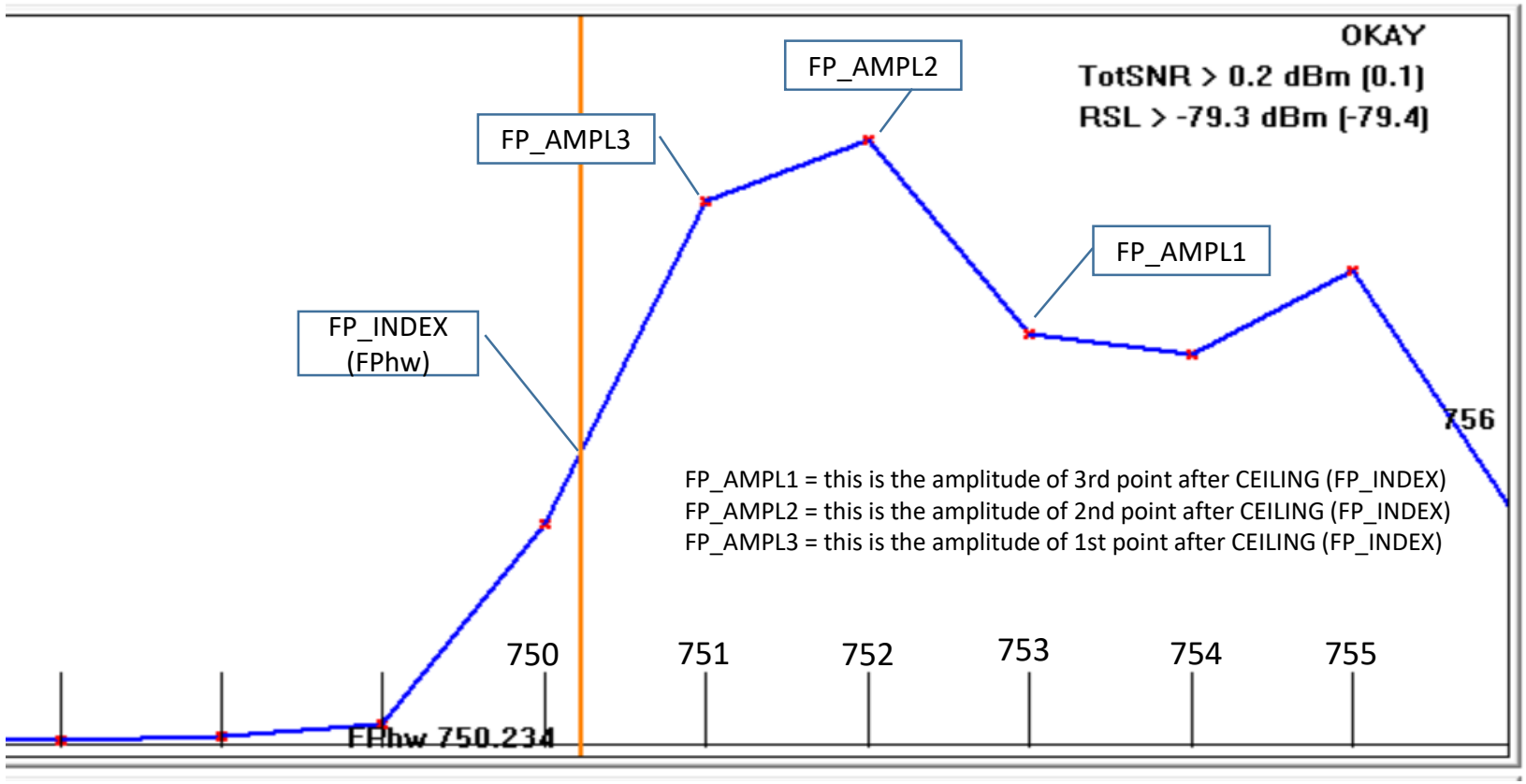
TX Frame TimeStamp Raw = 21 7DEBBE34
Adding Antenna Delay = 0021 7DEBBE34
05 Tx time = 2.251203838954828e+000

Rx time is the time of reception of a frame - decimal is the DW1000 time converted to second the DW1000 time (40 bit number)
Rx time(un) is the raw time stamp before any DW1000 time adjustments after first path calcu LDE
txdly and **rxdly** are the TX and RX antenna delays as programmed
RXDATA: these are the received bytes
RX OK - this signifies good reception
HLP - this is first path index in the accumulator
PSC - number of accumulated preamble symbols
NTH* - noise threshold
T - temperature and voltage - read from DW1000 on frame reception
RSL** - received signal level (dBm) - calculated as given by the formula in User Manual
FSL - first path signal level (dBm) - calculated as given by the formula in User Manual
Accum Len 1016 - these are the real and imaginary parts of the accumulator CIR for the rece frame

Tx time is the time of the frame transmission (has TX antenna delay added)

*the LDE computes the threshold based on the noise / signal found in the 1st 200-300 samples of the accumulator. The level of noise depends on various HW and environmental factors.
(See *APS006 Part 3 DW1000 Diagnostics for NLOS Channels*)

**RSL is the receive signal level (dBm) - see User Manual section 4.7 Assessing the quality of reception and the RX timestamp



After research and investigation we decided that the chip algorithm should locate the bulk of the channel between index 728 and 855 of the CIR memory. So the first path tends to end up around 740-750.

Other relevant documentation:

- APS006 part 1 channel effects on range accuracy
- APS006_Part2 NLOS Operation and Optimizations
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- PC Decaranging Source Code**

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** Available at request

Register 0x12: contains FP_AMP2 and FP_AMP3 - the FP_AMP3 is the **1st point after FP**,
Register 0x15: contains FP_AMP1 which is the **3rd point after FP**

The DW1000 algorithm that processes the accumulator samples does not use the raw sample values as you see when you read the accumulator. It uses samples after DC offset estimate is removed. Also the magnitude calculated by DW1000 algorithm is an approximation, the sqrt function is not used.