

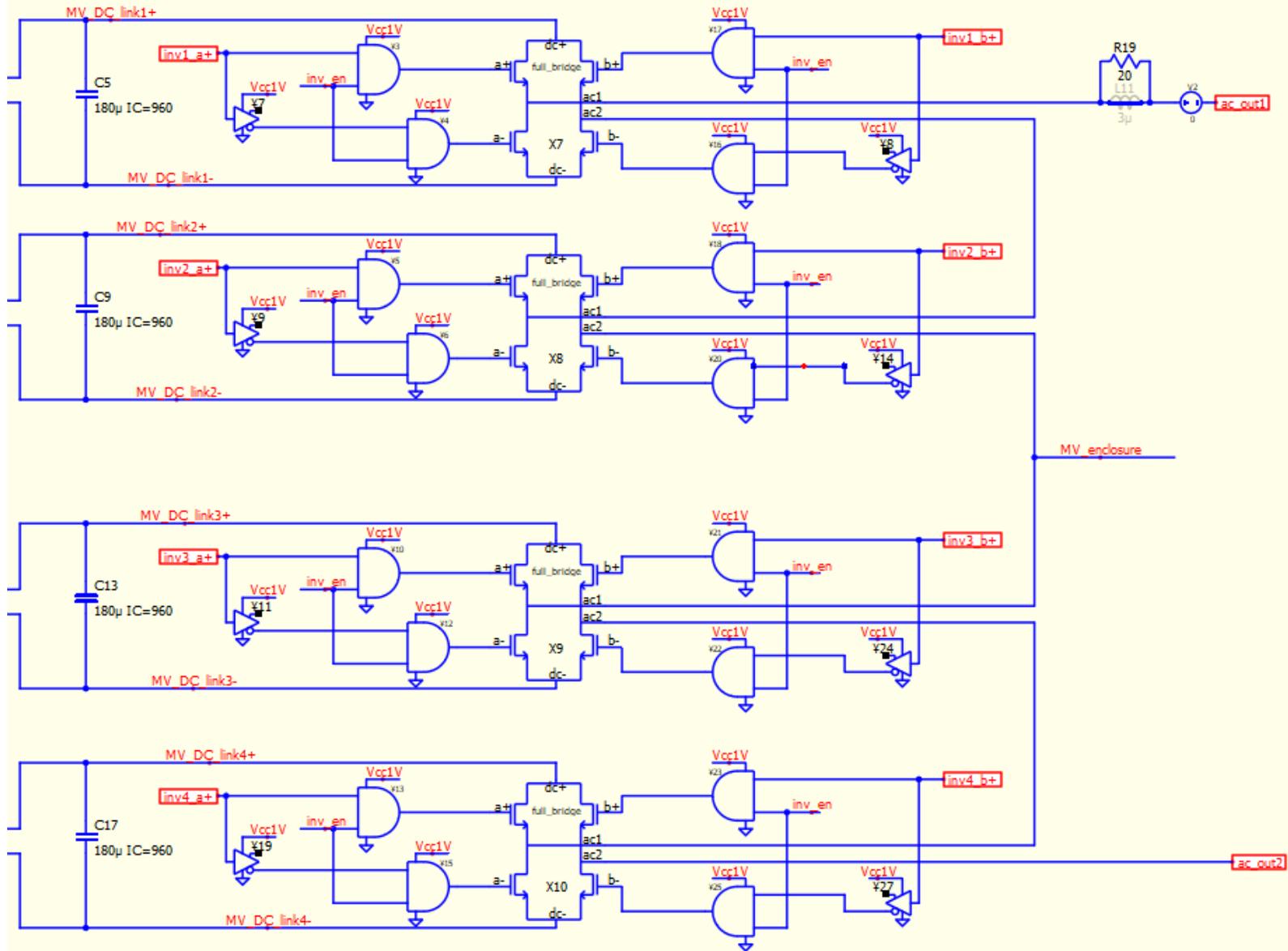
Hi,

I encounter very strange simulation artefact, and I would be thankful if you could assist. I simulate a rectifier in a close loop.

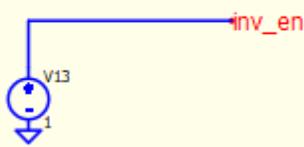
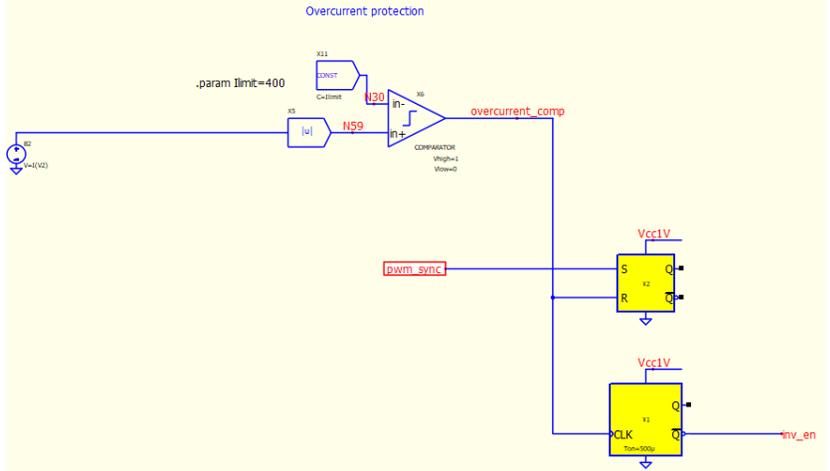
In the rectifier I simulate, I have the overcurrent protection that enables/disables the full bridges, and I simulate two cases: (a) no overcurrent protection, and (b) with overcurrent protection. The strange part is that the ac grid currents are different and are very distorted when I simulate the circuit with the OC protection, even though the current does not reach the OC protection limit! Moreover, if the considered power block includes some logic, whose outputs are not connected to anything, the ac grid currents are also impacted!!!

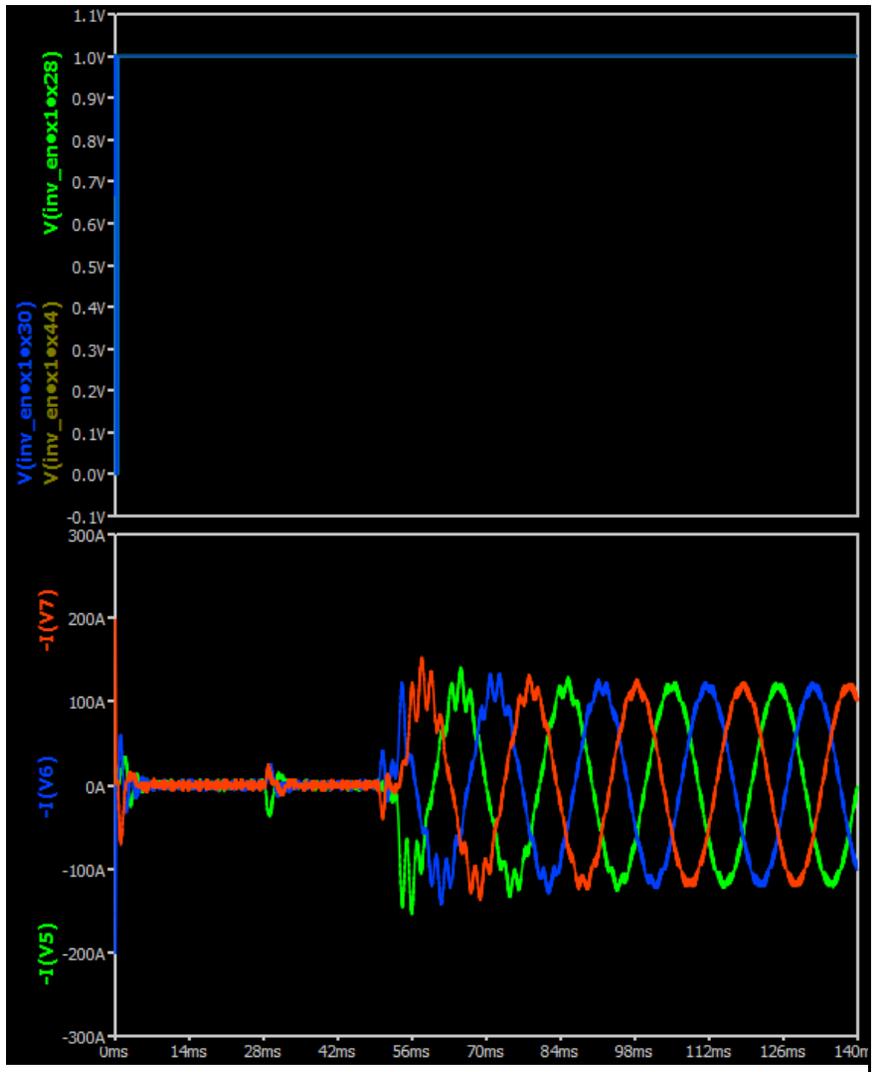
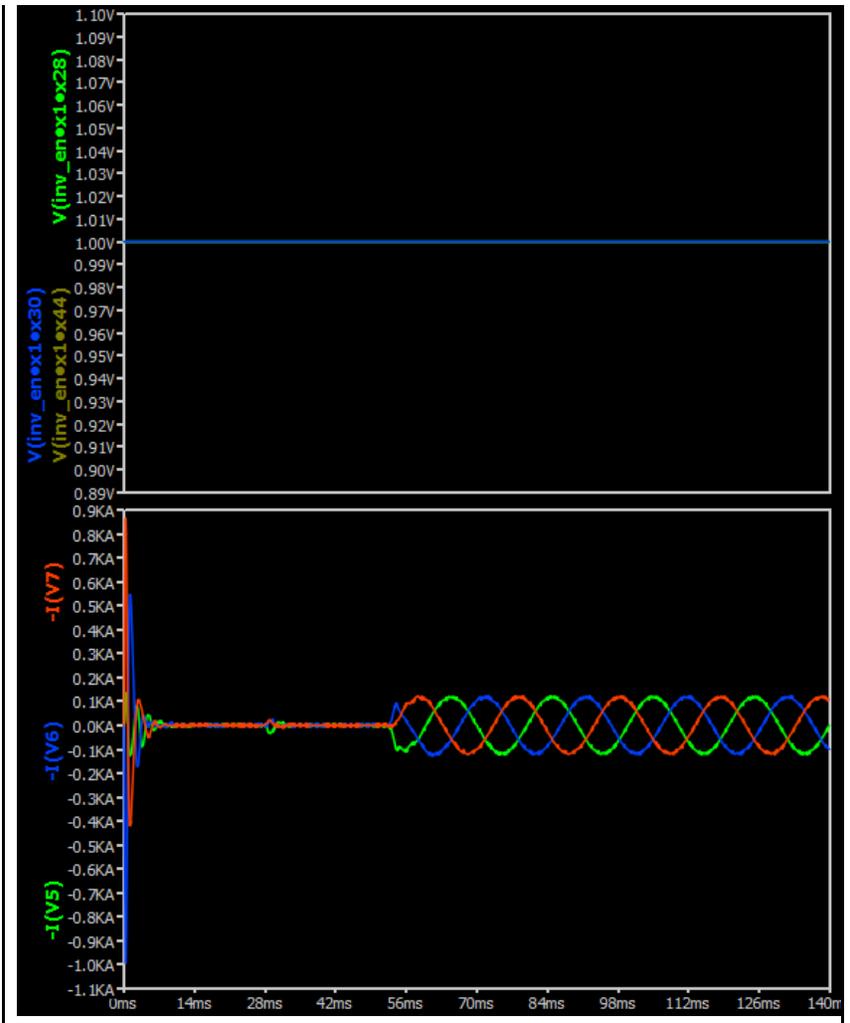
Therefore, I think that it is a simulation artefact.

The top level schematic is MV_converter_6cells_closed_loop_v3.qsch. The considered block is single_power_module_w_ideal_dc_xfrm.qsch, and the enable/disable of the bridges is shown as follows:



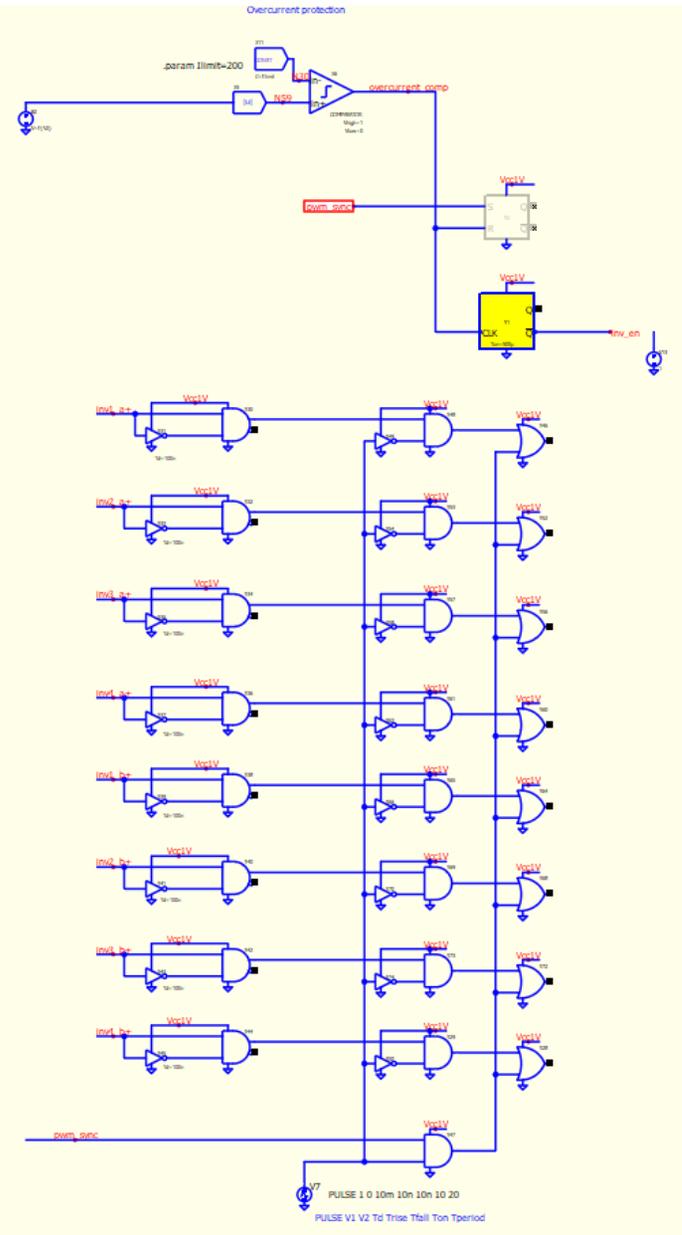
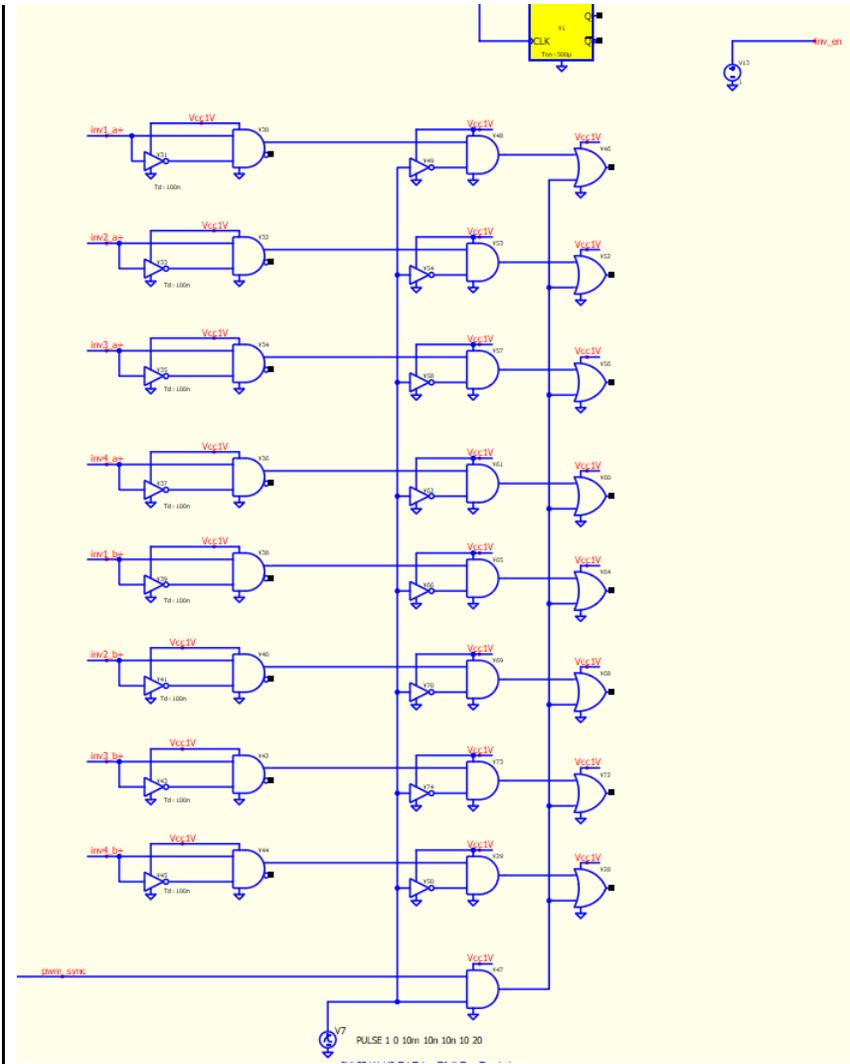
The following table shows the two configuration (without the additional logic) and the results. The left column in the table below shows the ac currents without the OC protection, and the right column shows the same currents with the OC protection. The protection is set at 200 A, and it can be seen that the current does not reach the tripping point, except at the very beginning of the simulation. Until t=50 ms, the current should be very low, as the load of the rectifier is at high-Z.

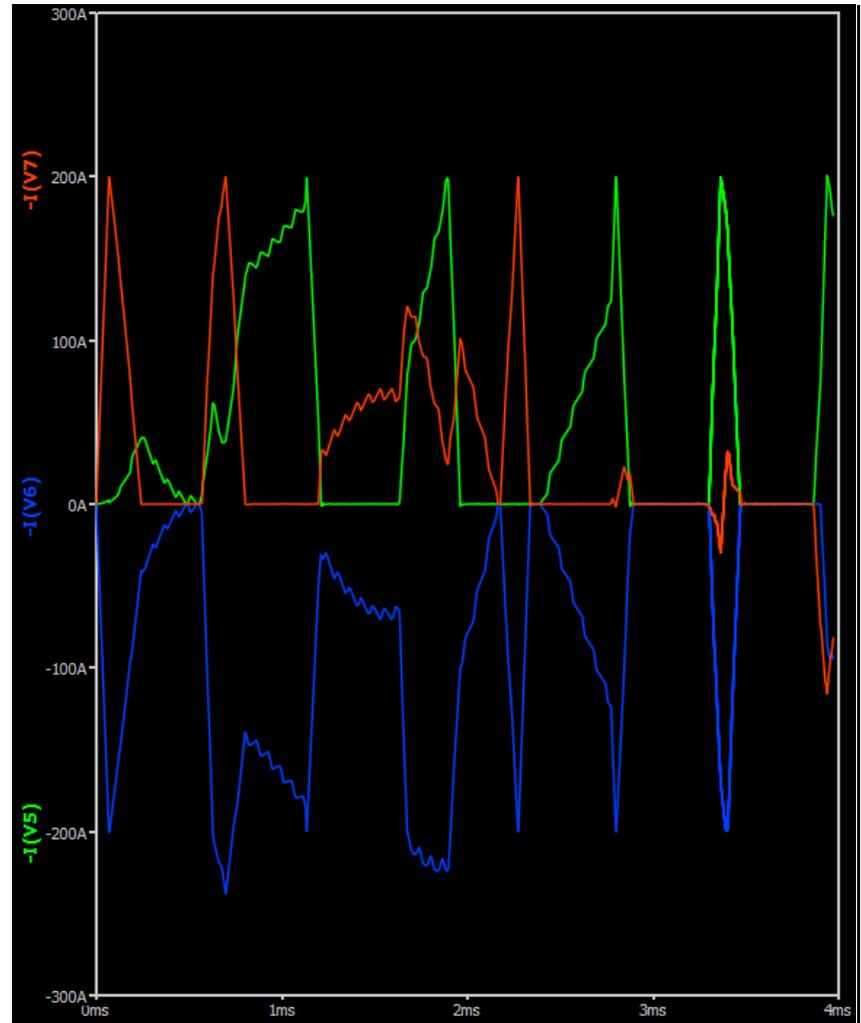
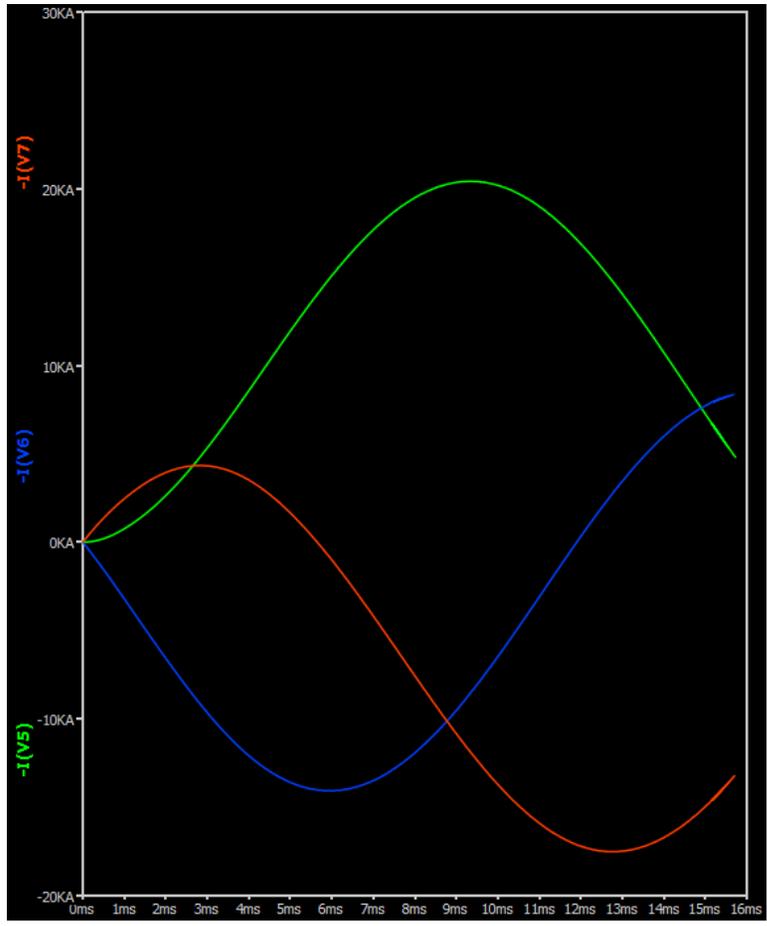
No overcurrent protection	With overcurrent protection
 <p>A simple circuit diagram showing a voltage source labeled V13 connected to a node labeled 'inv_en'.</p>	 <p>A detailed circuit diagram for overcurrent protection. It includes a current sensor N59 with a gain of 1000 and a limit of 400. The sensor output is connected to a comparator labeled 'overcurrent_comp'. The comparator's output is connected to the S input of a flip-flop (X2) and the CLK input of a timer (X1). The flip-flop's Q output is connected to the 'inv_en' signal. The timer has a time constant of 100µs. The circuit is powered by Vcc1V and includes a 'pwm_sync' input.</p>



The next table shows the situation when the same `single_power_module_w_ideal_dc_xfrm.qsch` block has a logic circuit whose outputs are not connected to anything, the AC grid currents are totally different as shown below. This logic was supposed to be a part of the overcurrent protection, but its outputs are disconnected.

No overcurrent protection + disconnected logic	With overcurrent protection + disconnected logic
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Thank you very much,

Nikolay